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Use Cases

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Use Cases

Custom silicon and tailored system-on-chip (SoC) designs can unlock significant value across many industries and application domains.

Autonomous-Vehicle Perception Engine

- **What the customer builds:** An on-board perception processor that fuses LiDAR, radar, and camera streams and runs a YOLO-v8 object-detection model at 120 fps.
- **Why custom silicon:**
  - Integrated multi-modal AI accelerator + safety-monitored Cortex-M core → sub-10 ms end-to-end latency, < 5 W power.
  - Meets ISO 26262 ASIL-D functional-safety requirements (hard-wired watchdog, lockstep cores).

Wearable Continuous-Glucose Monitor (CGM)

- **What the customer builds:** A skin-adhesive patch that measures interstitial glucose, processes the signal, encrypts the data, and transmits via BLE.
- **Why custom silicon:**
  - Ultra-low-power analog front-end + on-die DSP for filtering → < 30 µW active consumption.
  - Secure element integrated for HIPAA-grade encryption, eliminating an external MCU.

Data-Center AI Inference Accelerator

- **What the customer builds:** A rack-mount inference card that serves transformer-based language-model queries for a SaaS chatbot.
- **Why custom silicon:**
  - Systolic-array matrix engine delivering 250 TOPS/W, 40 % lower TCO vs. GPU-based servers.
  - Built-in TLS-offload and secure key vault, removing separate network-security appliances.

5G Small-Cell Baseband Processor

- **What the customer builds:** A compact indoor small cell that supports sub-6 GHz and mmWave bands, handling beamforming and carrier aggregation.
- **Why custom silicon:**
  - Integrated RF front-end + baseband DSP on a single die → < 10 mm^2 footprint, 20 % lower BOM cost.
  - Deterministic processing guarantees < 1 ms scheduling latency for URLLC (ultra-reliable low-latency communication).

Premium Smartphone AI Camera Pipeline

- **What the customer builds:** A flagship phone camera that does on-device HDR-plus, night-mode, and real-time portrait segmentation without sending data to the cloud.
- **Why custom silicon:**
  - Dedicated ISP + AI NPU (8 TOPS) on the same SoC → 3× faster RAW-to-JPEG pipeline, < 200 ms total capture-to-share time.
  - Power-gating of NPU when idle saves > 30 % battery versus a CPU-only solution.

Secure Edge Router with On-Chip Encryption

- **What the customer builds:** An industrial edge router that terminates TLS, performs DPI, and enforces zero-trust policies for a factory floor.
- **Why custom silicon:**
  - On-die AES-256/GCM engine + post-quantum KEM accelerator → > 10 Gbps encrypted throughput with < 5 ns per packet latency.
  - Hardened boot and tamper-detect logic meet IEC 62443 security class 4.

How Customers Typically Approach a Custom-Silicon Project [MATCH THIS WITH WHAT WE CAN OFFER AT MOTIUS AND HOW WE PLAY A KEY ROLE HERE]

- **Define the Value Proposition** – Identify the metric that matters most (e.g., power per inference, latency, cost per unit, security level).
- **Benchmark Off-The-Shelf Alternatives** – Quantify the gap between existing components and the target metric.
- **Select an Architecture Partner** – Choose a foundry/ASIC design house that offers the required process node, IP libraries, and design-for-test capabilities.
- **Co-Design IP Blocks** – Work with the partner to create or adapt cores (AI acelerator, DSP, RF front-end, secure enclave) that meet the spec.
- **Prototype & Validate** – Fabricate engineering samples, run silicon validation, and iterate on firmware/software stacks.
- **Scale to Volume** – Optimize for yield, test coverage, and supply-chain logistics before mass production.

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