MOTIUS

WE R&D.

Commercial RISC-V Platform

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November 19, 2025 20:31 (ccd1cd0)

Commercial RISC-V Reference Platform

Current Active Commercial Project (2025)

Trade Show Demonstrator in Development

Supporting a commercial RISC-V IP provider in developing a reference platform integration for their first RISC-V processor on FPGA. This integration serves as a demonstrator for trade shows, client engagements, and sales activities.

Project Overview

Client: Commercial RISC-V IP Provider (Confidential)

Timeline: Q1 2025 - Today (Ongoing)

Type: Commercial RISC-V integration project

Objective: Build a functional and scalable reference integration of the client's RISC-V processor IP, including essential peripherals and development infrastructure, on FPGA hardware.

Project Goals

Build a functional and scalable reference integration showcasing:

- The client's RISC-V processor IP capabilities
- Complete peripheral ecosystem
- Development tools and workflows
- Demo applications for trade shows and customer engagement
- Technical reference for client internal teams

Key Deliverables

CPU Integration

Dual RISC-V CPU Architecture:

- **Andes RISC-V CPU** - Commercial RISC-V core integration
- **Synopsys RISC-V CPU (ARC-V)** - Additional commercial core
- Validation of both CPU cores on FPGA platform
- Performance benchmarking and optimization

Peripheral Integration

Complete System-on-Chip Ecosystem:

- [x] DDR memory controller integration
- [x] SRAM interfaces
- [x] UART (serial communication)
- [x] SPI (Serial Peripheral Interface)
- [x] I^2C (Inter-Integrated Circuit)
- [x] JTAG debug interfaces
- [x] GPIO (General Purpose I/O)
- [x] AXI and Wishbone bus architectures

Development Infrastructure

Automated Workflows:

- [x] FPGA synthesis automation
- [x] Deployment workflows
- [x] Verification and testing frameworks
- [x] Continuous integration pipelines

Bootloader & System Software

- [x] Initial bring-up of bootloader
- [x] Device tree configuration
- [x] Driver development for peripherals
- [x] Demo application development

Documentation & Support

- [x] Technical documentation for client teams
- [x] Integration guides
- [x] Reference designs
- [x] Customer demonstration materials

FPGA Platforms

Platform	Series	Usage
AMD Xilinx Kintex-7	7-Series	Primary development platform (Genesys 2)
AMD Xilinx Ultrascale+	Ultrascale	Advanced features and performance

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Technologies & Tools

Hardware

- **Genesys 2** – AMD Kintex-7 development board
- **Ultrascale+** – High-performance FPGA platform
- Multiple I/O interfaces for peripheral connectivity

IP Cores

- **Andes RISC-V CPU** – Commercial processor IP
- **Synopsys RISC-V CPU (ARC-V)** – Additional processor option
- **Synopsys Peripheral IPs** – Commercial IP building blocks
- **Open-source modules** – UART, SPI, I^2C, AXI, Wishbone

Development Tools

- **Open-source toolchains** – Compiler, debugger, simulator
- **Vivado Design Suite** – FPGA synthesis and implementation
- **Segger debuggers** – JTAG debugging infrastructure
- **Custom automation scripts** – Build and deployment workflows

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Project Approach

Phase 1: Requirements & Architecture

- Analysis of client CPU IP specifications
- System architecture design
- Peripheral selection and planning
- Resource estimation and planning

Phase 2: Core Integration

- RISC-V CPU integration into FPGA
- Validation of CPU functionality
- Performance testing and optimization
- Debug infrastructure setup

Phase 3: Peripheral Ecosystem

- Memory controller integration (DDR, SRAM)
- Communication interfaces (UART, SPI, I^2C)
- Bus architecture (AXI, Wishbone)
- GPIO and debug interfaces (JTAG)

Phase 4: System Software

- Bootloader development
- Device tree configuration
- Driver development

- Operating system bring-up

Phase 5: Demo & Documentation

- Demo application development
- Performance benchmarking
- Technical documentation
- Trade show preparation

Current Status

> **Active Development (2025)**
>
> **Status:** In progress
>
> **Completed:** - Andes RISC-V CPU integration ✅ - Synopsys RISC-V CPU integration ✅ - Core peripheral set integrated ✅ - Bootloader and device tree operational ✅ - Automated synthesis workflows ✅
>
> **In Progress:** - Demo application development 🔄 - Documentation finalization 🔄 - Trade show preparation 🔄

Technical Achievements

Dual CPU Architecture

Successfully integrated two different commercial RISC-V cores on the same platform:

- Demonstrates flexibility of RISC-V ecosystem
- Allows direct comparison of different IP options
- Provides customers choice based on their requirements

Comprehensive Peripheral Set

Complete system-on-chip functionality:

- Memory hierarchy (DDR, SRAM)
- Standard communication protocols
- Debug and development infrastructure

- Extensible for customer-specific peripherals

Automated Workflows

Production-ready development environment:

- One-command FPGA synthesis
- Automated testing and verification
- Continuous integration ready
- Reproducible builds

Value to Client

Customer Engagement

- **Trade show demonstrations** – Working RISC-V system for exhibitions
- **Customer evaluations** – Reference platform for potential clients
- **Sales support** – Proven implementation to accelerate deals

Technical Validation

- **IP validation** – Proves CPU IP works in real systems
- **Performance data** – Benchmarks for customer presentations
- **Integration knowledge** – Documents how to use their IP

Documentation & Support

- **Reference design** – Starting point for customer implementations
- **Integration guides** – How to use client IP effectively
- **Technical support** – Documentation for internal teams

Lessons & Best Practices

Multi-Core Integration

- Handling multiple RISC-V cores requires careful architecture planning
- Vendor-specific peripherals need adaptation for different CPUs
- Debug infrastructure must support multiple cores

Commercial IP Integration

- Working with commercial IP providers requires:
- Understanding licensing and usage terms
- Coordinating with vendor support teams
- Managing IP updates and versions
- Documentation and knowledge transfer

Reference Platform Development

- Must balance:
- Comprehensive features vs. simplicity
- Performance vs. resource usage
- Flexibility vs. ease of use
- Documentation completeness vs. timeline

Impact on Motius Capabilities

This project strengthens our:

Commercial RISC-V Experience: - Proven ability to integrate commercial IP (Andes, Synopsys) - Established relationships with major IP providers - Understanding of commercial IP workflows

Multi-Core Systems: - Experience with multiple RISC-V cores on single platform - Comparative analysis of different RISC-V implementations - Architectural decisions for multi-core systems

Customer-Facing Deliverables: - Trade show demonstration experience - Reference platform development methodology - Technical documentation best practices

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← Game Engine Chip **Next: eMil Project →**