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WE R&D.

Game Engine Chip - Manufactured Silicon

Motius GmbH

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Game Engine Chip - Our First Manufactured Silicon

Complete ASIC Lifecycle: FPGA → Tape-Out → Manufacturing → Testing

> **Successfully Manufactured Silicon (2022-2024)**
>
> Motius's first custom chip - from FPGA prototype to manufactured silicon. Submitted for manufacturing in Q3 2022/Q1 2023, received 40 working chips in April 2024.

Project Overview

Objective: Design, manufacture, and validate a complete game engine (Pong) implemented in custom silicon

Timeline: Q1 2022 - Q4 2024 (33 months)

Result: 40 manufactured chips in M.2 QFN package, successfully tested and validated

The manufactured Game Engine chip in M.2 module format - "F2" marking shows efabless fabrication

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The Complete Journey

Phase 1: FPGA Prototype (Q1-Q2 2022)

Goal: Prove the concept works in hardware

Complete Game Engine in HDL

Designed and implemented the entire Game Engine game in hardware description language

VGA/HDMI Video Output

Real-time game display rendering with full timing control

Proximity Sensor Input

ST ToF (Time-of-Flight) sensor for player controls

Physics in Hardware

Game logic, collision detection, and scoring implemented in FPGA

Platform: AMD Xilinx Artix-7 FPGA (Nexys A7, Arty A7-100T boards)

Result: Working game engine running entirely in FPGA hardware

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Phase 2: Tape-Out Preparation (Q3 2022 - Q1 2023)

Goal: Prepare the design for manufacturing

The Challenge: Google/efabless offered free chip manufacturing through their open-source program, but the Caravel toolchain was pre-alpha with minimal documentation.

What We Learned	What We Did
Manufacturing design rules (PDK compliance)	Figured out the Caravel toolchain from scratch
Standard cell library requirements	Understood foundry component requirements
Voltage configuration and pin planning	Design rule checking and layout verification
Design-for-manufacturability principles	Prepared final submission for fabrication
Verification against foundry constraints	Navigated pre-alpha tools with limited docs

Result: Successfully submitted design to efabless/Google open-source manufacturing program

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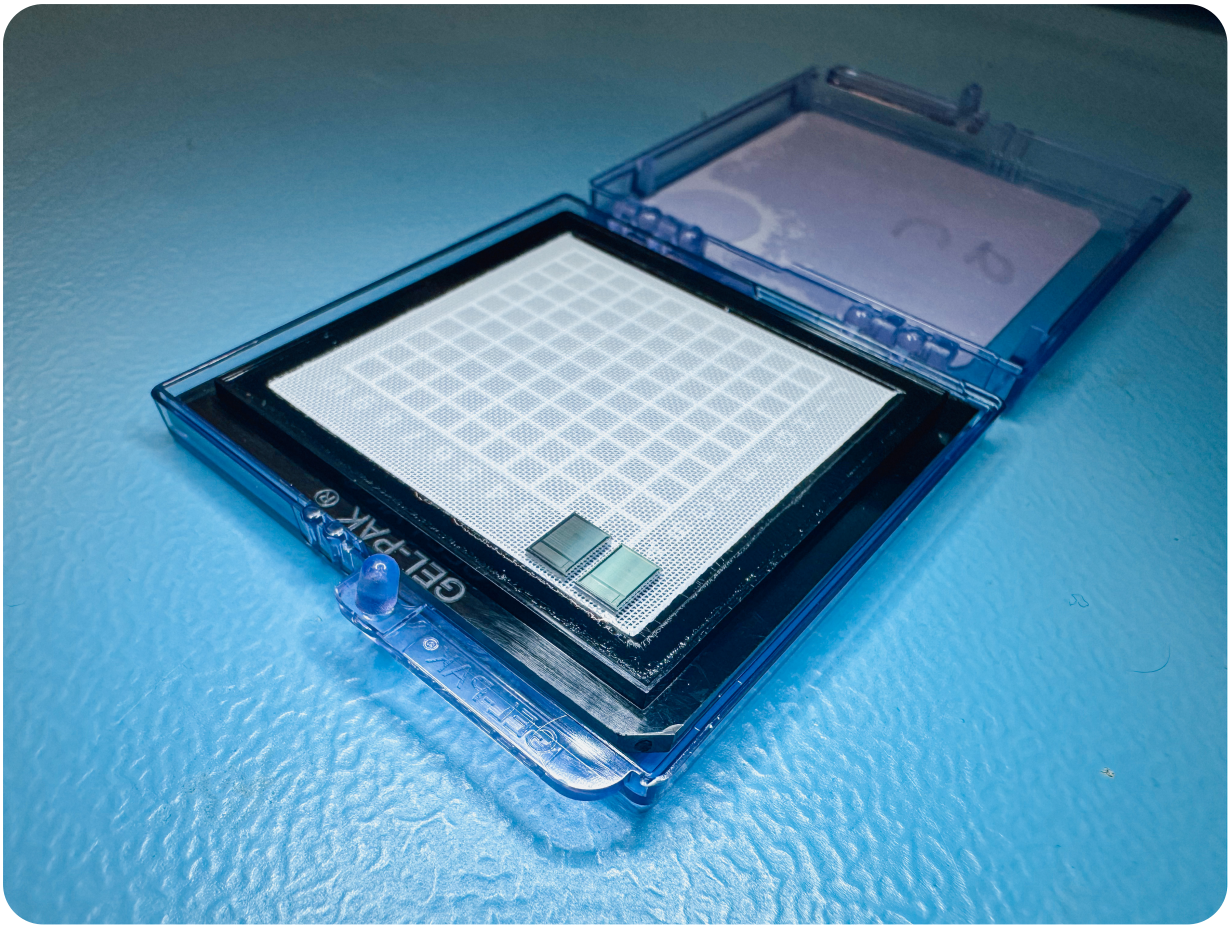
Phase 3: Manufacturing & Testing (2023-2024)

The Wait: Nearly 2 years from submission to receiving chips. This is typical for pilot programs and shuttle runs. Many designs never get manufactured - ours did!

April 2024: Chips Arrived!



Opening the package reveals the actual silicon die - our custom game engine on real silicon

We received 40 chips in M.2 QFN package format with our design on actual silicon!

The Debug Challenge: Testing revealed an issue - VGA video worked perfectly ✅ but ToF sensor didn't respond ❌

❗ The Problem

Pins connecting the ToF sensor were configured to the wrong voltage level during manufacturing. This was a configuration issue, not a functional logic problem.

✔ The Solution

Instead of the chips becoming unusable, we modified the external interface electronics to match the voltage levels the pins provided. **Successfully brought the Game Engine chip to life!** 🚀

Phase 4: Production Board (Planned)

Next Step: Design a card-sized custom PCB integrating all 40 chips to showcase our hardware design capabilities and provide a physical demonstration of manufactured silicon at scale.

Key Components Developed

Display Controller

Custom VGA/HDMI video output controller for game rendering with full timing control

Collision Detection

Hardware-accelerated physics engine and collision detection in real-time

Rendering Pipeline

Complete graphics rendering pipeline implemented in silicon

Game Logic

Full game engine logic, scoring, and difficulty progression in hardware

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Technologies & Tools

Phase	Technology
FPGA Prototype	AMD Xilinx Artix-7 (Nexys A7, Arty A7-100T)
HDL	Verilog/SystemVerilog

Custom IP	Complete game engine (designed by Motius)
Sensors	ST ToF proximity sensor for player input
Tape-Out Tools	Google Caravel (open-source), efabless platform
Foundry	Google/efabless open-source shuttle program
Package	M.2 QFN form factor
Deliverable	40 manufactured chips, tested and validated

What We Learned

This project demonstrated the complete silicon development lifecycle. Here are the key insights:

PDK Compliance is Critical

Manufacturing rules must be followed precisely. This is completely different from functional correctness in FPGA.

Voltage Configuration Matters

Pin voltage levels must match peripheral requirements. Configuration errors can make chips unusable, but some issues can be worked around externally (as we did).

Testing is Essential

Manufactured silicon may have defects. Post-silicon validation is time-intensive but critical for finding and recovering from issues.

Timeline Reality: 18-24 Months

From submission to working chips is real, not theoretical. Manufacturing is an arduous process - be prepared for the wait.

Manufacturing ≠ Functionality

The manufacturing phase is about using manufacturing rules correctly. Many things can go wrong beyond your design logic.

Why This Matters

Most semiconductor consultants fall into two categories:

FPGA specialists never cross into actual silicon manufacturing. **ASIC designers** work for design houses but don't own the full lifecycle.

Motius has proven end-to-end capability:

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Requirements → Design → FPGA Validation → Tape-Out → Manufacturing → Tested Silicon
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This experience is invaluable for ASIC preparation projects.

What This Means for Your Project

Real Experience

We've submitted designs for tape-out, waited through manufacturing, debugged manufactured silicon, and recovered from manufacturing defects.

Accurate Timelines

We understand real timelines (18-24 months), not theoretical ones. Better preparation means realistic expectations.

De-Risked Process

Proven relationships with manufacturing partners (Google/efabless). We know what foundries actually need and how to navigate issues.

Complete Lifecycle

From requirements to tested silicon, we've done it. We can guide you through every phase of ASIC development.

Open Source

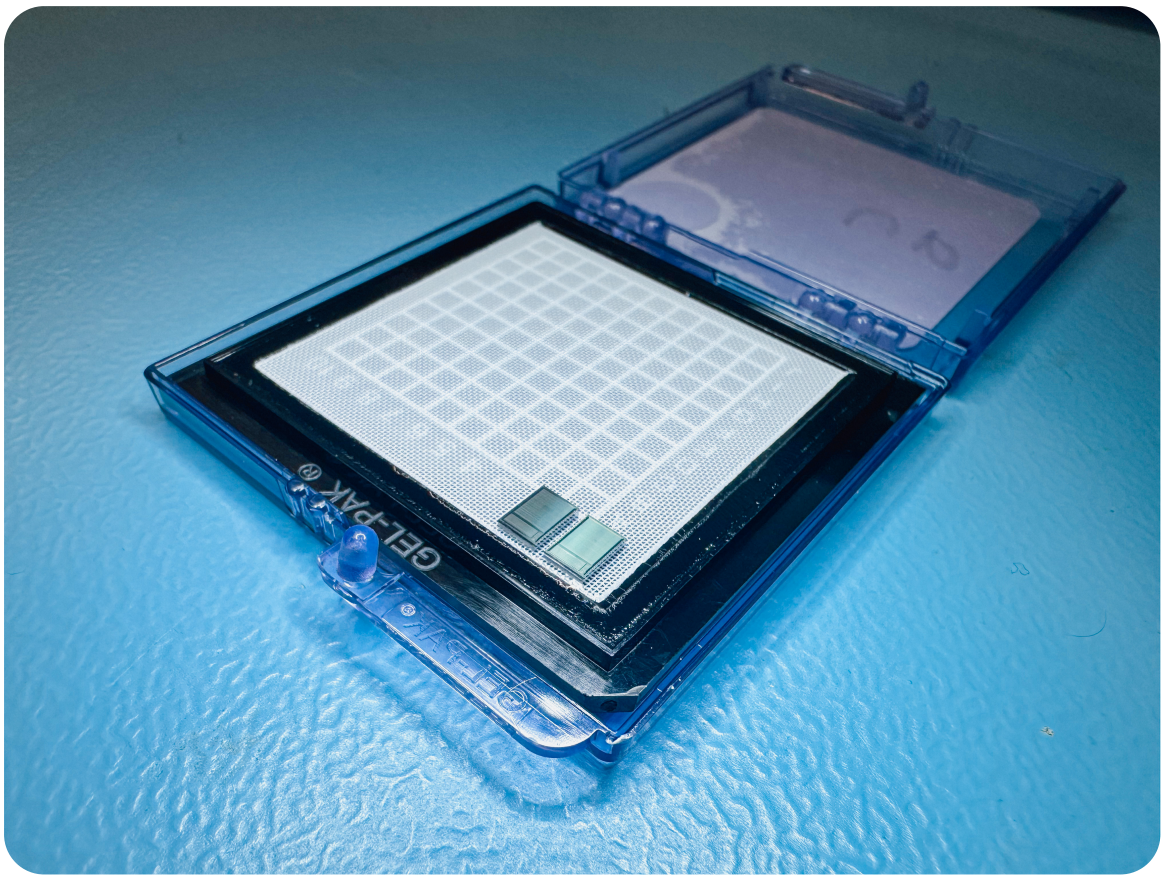
Repository

The Game Engine chip design is open-source:

GitHub: github.com/motius/ge-chip

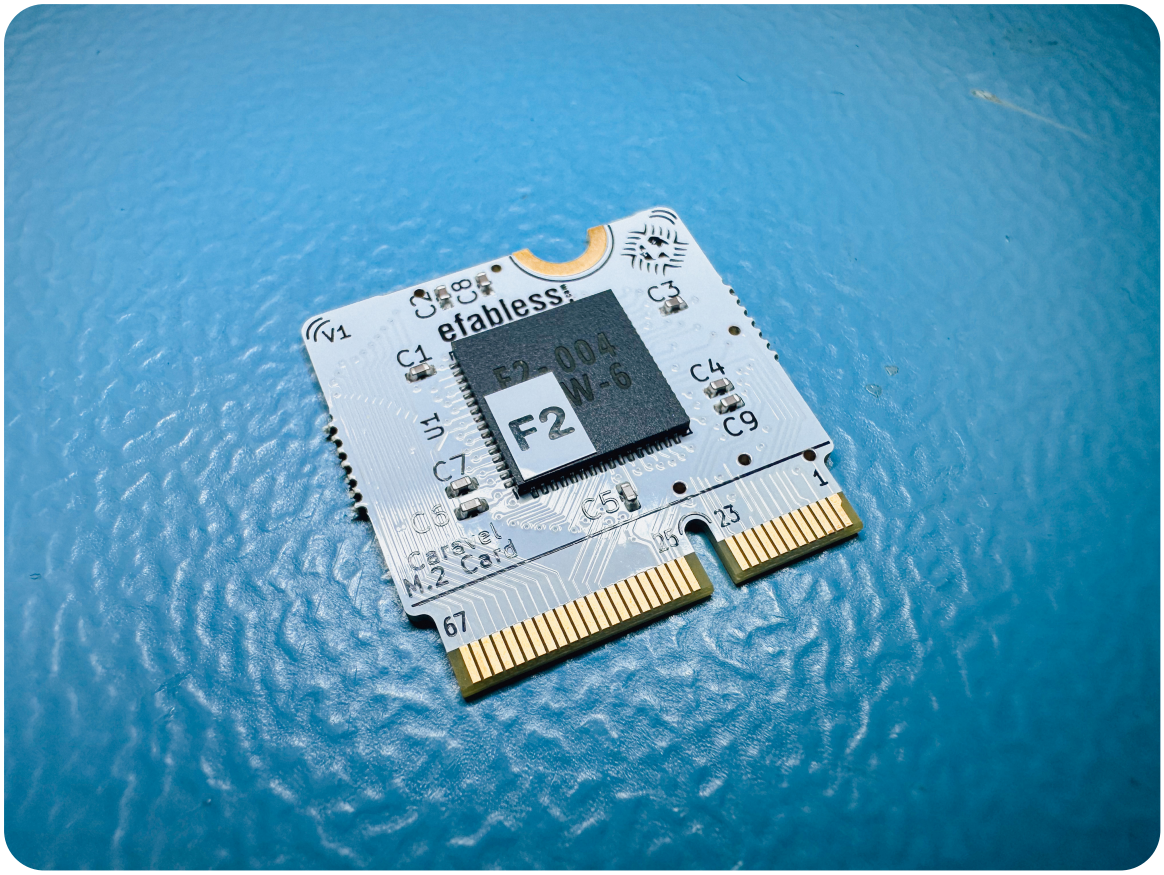
The Manufactured Result

Manufactured Silicon



Actual silicon die visible inside the QFN package

M.2 Module Format



Production-ready M.2 form factor with efabless fabrication

Status: 40 manufactured chips received, tested, and validated

Next Steps: Production board development to showcase all 40 chips on a single demonstration platform

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Next: Commercial Platform →