MOTIUS

WE R&D.

Our Approach

Motius GmbH

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Our Approach to Silicon Development

We bridge the gap between application requirements and manufactured silicon through proven FPGA prototyping and production integration expertise.

The Silicon Journey

Based on real experience manufacturing our own chip

Stage 1: Architecture Design (~6 months)

From requirements to working FPGA prototype with RISC-V CPU integration, custom IP development, and comprehensive validation.

System Specification

Define performance targets, power budgets, interface requirements, and peripheral ecosystem

HDL Implementation

Design in Verilog/VHDL with RISC-V CPU integration and custom IP cores

Simulation & Testing

Functional verification, timing analysis, and resource optimization

FPGA Prototyping

Working hardware demonstration on AMD Xilinx platforms

Tools & Technologies: Vivado, Synplify, Design Compiler, Precision FPGA Synthesis, Questa One Sim

Key Deliverables: System architecture specification, synthesizable HDL code, validated FPGA prototype, test suite and documentation

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Stage 2: Physical Design (~4 months)

ASIC-ready design with PDK compliance, timing closure, and tape-out preparation.

Floorplanning & Placement

Strategic placement of functional units, memory blocks, and I/O pads

Tapeout Verification

DRC/LVS checks, timing closure, and manufacturing rule compliance

PDK & Standard Cells

Process Design Kit verification and standard cell library integration

Manufacturing Prep

GDSII generation, documentation package, foundry submission files

Tools & Technologies: PrimeTime, Innovus Implementation System, foundry-specific PDKs

Key Deliverables: Floorplan layout, verified GDSII files, timing reports, manufacturing documentation

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Stage 3: Manufacturing & Testing (~4 months coordination | 18-24 months actual)

Foundry coordination, manufacturing oversight, and post-silicon validation.

Foundry Coordination

IC manufacturing management with wafer selection and die packaging

Silicon Production

Wafer fabrication, die cutting, packaging, and assembly

Post-Silicon Testing

Electrical validation, functional testing, and defect analysis

Debug & Recovery

Issue identification and mitigation strategies for manufacturing defects

Manufacturing Partners:

Region	Partners
German/EU	Fraunhofer IIS, RoodMicrotec, Racyics, TES Electronic Solutions, iC-Haus, Infineon
Global Foundries	TSMC, Samsung, GlobalFoundries
Open-Source	Google/efabless shuttle programs

Reality Check: 18-24 months from submission to working chips (we know because we've done it before)

Key Deliverables: Manufactured chips, test reports, characterization data, production-ready design

Service Offerings

RISC-V FPGA Platform Development

€100-200K | 4-6 months

Working FPGA reference platform with RISC-V CPU, peripherals, and demo applications

Custom IP Core Development

€80-150K | 3-5 months

Hardware-accelerated IP cores (FFT, CRC, ML acceleration) integrated and verified

FPGA-to-ASIC Preparation

€150-300K | 4-6 months

ASIC-ready design with feasibility study, partner introduction, and tape-out prep

Requirements Engineering

€40-80K | 6-10 weeks

Feasibility report with business case, architecture options, and implementation roadmap

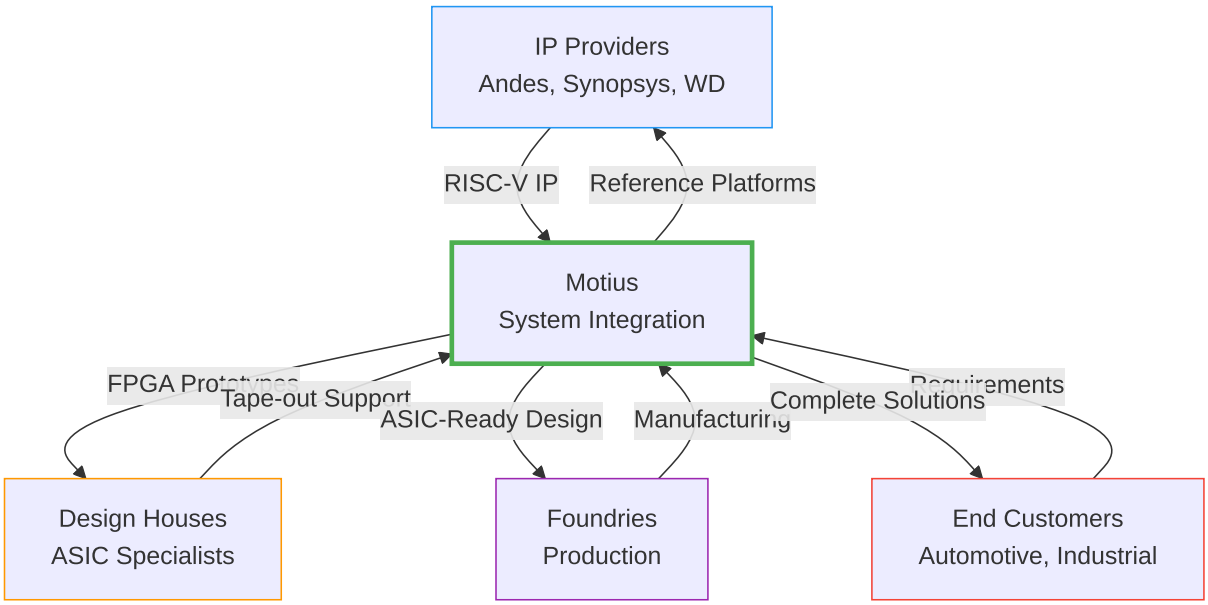
Production Integration

€200-400K | 8-12 months

Production-ready hardware with CE, EMC, and safety certifications (IEC 61508 SIL2)

Partnership Model

We work with (not against) the ecosystem



Why Work With Us

We've Manufactured Our Own Chip

Real tape-out experience, debugged manufacturing defects, understand true timelines

Multi-Vendor RISC-V Experience

Proven with Andes, Synopsys ARC-V, Western Digital cores across multiple platforms

Production-Ready Systems

2M+ units shipped, CE/EMC certified, IEC 61508 SIL2 functional safety experience

Full-Stack Capability

From application requirements → FPGA → ASIC → production hardware → certifications

Who We Work With

Customer Type	How We Help
Automotive & Industrial Companies	Evaluate if custom silicon makes business sense, FPGA prototyping to de-risk decisions, production integration with certifications
IP Providers & SoC Designers	Reference platform development, customer demonstration support, application expertise

Sweet spot: Mid-size manufacturers (€50M-500M revenue), 5,000-50,000 units/year

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